Claims:

1. A method of forming an electrical interconnect in a semiconductor device comprising:

providing a substrate having two or more transistors with active areas therebetween, the transistors having gate regions wherein the gate regions are not exposed;

creating an insulating layer overlying the transistors and the active areas;

forming a contact plug/interconnect opening over a first active area and a portion of a first transistor immediately adjacent the first active area;

forming a dielectric material spacer within the contact plug/interconnect opening thereby forming two contact holes;

removing insulating material overlying one or more of the active areas including the first active area such that the active areas are exposed;

exposing a portion of the gate region of the first transistor; and

depositing interconnect material within the contact plug/interconnect opening on the exposed portion of the gate region of the first transistor and the first active area thereby electrically connecting the first transistor to the first active area.

2. The method of claim 1, wherein the dielectric material spacer comprises TEOS or silicon dioxide.

3. The method of claim 1, wherein the transistors are FET transistors.

4. The method of claim 1, wherein the FET transistors are shallow-trench isolated FET transistors

5. A method of forming electrical interconnects in a semiconductor device comprising:

providing a substrate having two or more transistors with active areas therebetween, the transistors having gate regions wherein the gate regions are not exposed;

creating an insulating layer overlying the transistors and the active areas;

forming one or more contact plug openings within the insulating layer over one or more of the active areas (such that a portion of the insulating layer remains overlying the active areas);

forming a contact plug/interconnect opening over a first active area and a portion of a first transistor immediately adjacent the first active area;

forming a dielectric material spacer within the contact plug/interconnect opening thereby forming two contact holes and a layer of dielectric material over the active areas;

removing insulating material overlying one or more of the active areas including the first active area such that the active areas are exposed;

exposing a portion of the gate region of the first transistor;

depositing interconnect material within the contact plug/interconnect opening on the exposed portion of the gate region of the first transistor and the first active area thereby electrically connecting the first transistor to the first active area; and

depositing interconnect material within the contact plug openings to form contact plugs to provide electrical connection to the one or more transistors.

6. The method of claim 5, wherein the dielectric material spacer comprises TEOS or silicon dioxide.

7. The method of claim 5, wherein the transistors are FET transistors.

8. A method of forming electrical interconnects in a semiconductor device comprising:

providing a substrate having two or more transistors with active areas therebetween, the transistors having gate regions wherein the gate regions are not exposed;

creating an insulating layer overlying the transistors and the active areas;

forming a contact plug/interconnect opening over a first active area and a first portion of a first transistor immediately adjacent the first active area;

forming a local interconnect trench over a second portion of the first transistor;

forming a dielectric material spacer within the contact plug/interconnect opening thereby forming two contact holes on either side of the spacer;

depositing dielectric material within the local interconnect trench;

removing insulating material overlying the first active area such that the first active area is exposed;

exposing the gate region underlying the first portion of the first transistor;

depositing interconnect material within the contact plug/interconnect opening onto the exposed first portion of the gate region of the first transistor and the first active area thereby electrically connecting the exposed portion of the gate region of the first transistor to the first active area; and

depositing interconnect material within the local interconnect trench to form a local interconnect to the first transistor.

9. The method of claim 8, wherein the dielectric material comprises TEOS or silicon dioxide.

10. The method of claim 8, wherein the transistors are FET transistors.

11. The method of claim 8, wherein the FET transistors are shallow-trench isolated FET transistors.

12. A method of forming electrical interconnects in a semiconductor device comprising:

providing a substrate having two or more transistors with active areas therebetween, the transistors having gate regions wherein the gate regions are not exposed;

creating an insulating layer overlying the transistors and the active areas;

forming one or more contact plug openings within the insulating layer over one or more of the active areas such that a portion of the insulating layer remains overlying the active areas;

forming a contact plug/interconnect opening over a first active area and a portion of a first transistor immediately adjacent the first active area;

removing insulating material overlying the active areas;

forming a dielectric material spacer within the contact plug/interconnect opening thereby forming two contact holes and a layer of dielectric material over the active areas;

removing insulating material overlying one or more of the active areas including the first active area such that the active areas are exposed;

exposing a portion of the gate region of the first transistor;

depositing interconnect material within the contact plug/interconnect opening on the exposed portion of the gate region of the first transistor and the first active area thereby electrically connecting the first transistor to the first active area; and

depositing interconnect material within the contact plug openings to form contact plugs to provide electrical connection to the one or more transistors.

13. The method of claim 12, wherein the dielectric material spacer comprises TEOS or silicon dioxide.

14. The method of claim 12, wherein the transistors are FET transistors.

15. The method of claim 12, wherein the FET transistors are shallow-trench isolated FET transistors.

16. A method for forming contact plugs and a contact plug/local interconnect in a semiconductor device, comprising:

providing a substrate having at least two transistors with gate regions each substantially covered with insulating caps, and active areas between adjacent transistors;

creating an insulating layer overlying the transistors and the active areas;

forming a mask overlying the insulating layer;

patterning the mask to define one or more contact plug openings over one or more of the active areas and to define a contact plug/local interconnect hole above a first transistor, a first portion of an immediately adjacent second transistor and a first active area between the first and second transistors;

removing the insulating layer at the contact plug openings and the contact plug/local interconnect hole and removing the insulating layer above the first portion of the second transistor;

forming a dielectric material spacer within the contact plug/interconnect hole above the first transistor;

forming a layer of the dielectric material over the active areas;

removing a portion of the insulating cap overlying the first portion of the second transistor thereby exposing a first portion of the gate region of the second transistor; and

depositing conductive material within the contact plug openings and the contact plug/local interconnect hole.

17. The method of claim 16, wherein the dielectric material comprises TEOS or silicon dioxide.

18. The method of claim 16, wherein the transistors are shallow-trench isolated FET transistors.

19. A method for forming contact plugs and a contact plug/local interconnect in a semiconductor device, comprising:

providing a substrate having at least two transistors with gate regions each substantially covered with insulating caps, and active areas between adjacent transistors;

creating an insulating layer overlying the transistors and the active areas;

forming a mask overlying the insulating layer;

patterning the mask to define one or more contact plug openings over one or more of the active areas and to define a contact plug/local interconnect hole above a first transistor, a first portion of an immediately adjacent second transistor and a first active area between the first and second transistors;

removing a portion of the insulating layer at the contact plug openings and the contact plug/local interconnect hole and removing the insulating layer above the first portion of the second transistor;

forming a spacer within the contact plug/interconnect hole above the first transistor;

forming a layer of the dielectric material over the active areas;

removing a portion of the insulating cap overlying the first portion of the second transistor thereby exposing a first portion of the gate region of the second transistor;

removing remaining portions of the insulating layer overlying the active areas; and

depositing conductive material within the contact plug openings and the contact plug/local interconnect hole.

20. The method of claim 19, wherein the dielectric material comprises TEOS or silicon dioxide.

21. The method of claim 19, wherein the transistors are FET transistors.

22. A method for forming contact plugs and a contact plug/local interconnect in a semiconductor device, comprising:

providing a substrate having at least two transistors with gate regions with insulating caps overlying the gate regions, and active areas between adjacent transistors;

creating an insulating layer overlying the transistors and the active areas;

forming a mask overlying the insulating layer;

patterning the mask to define one or more contact plug openings over one or more of the active areas, to define a contact plug/local interconnect hole above a first transistor, a first portion of an immediately adjacent second transistor and a first active area between the first and second transistors, and to define a local interconnect trench over a second portion of the second transistor;

removing the insulating layer at the contact plug openings, the contact plug/local interconnect hole, and the local interconnect trench, and removing the insulating layer above the first portion of the second transistor;

forming a dielectric material spacer within the contact plug/interconnect hole above the first transistor and at least partially filling the local interconnect trench;

removing at least a portion of the dielectric material spacer and at least a portion of the dielectric material in the local interconnect trench;

removing a portion of the insulating cap overlying the first portion of the second transistor thereby exposing a first portion of the gate region of the second transistor; and

depositing conductive material within the contact plug openings, the contact plug/local interconnect hole and the local interconnect trench.

23. The method of claim 22, wherein the dielectric material spacer comprises TEOS or silicon dioxide.

24. The method of claim 22, wherein the transistors are FET transistors.

25. A method for forming contact plugs and a contact plug/local interconnect in a semiconductor device using a single mask, the method comprising:

providing a substrate having at least two FET transistors with insulating caps overlying the gate regions, and active areas between adjacent transistors;

creating an insulating layer overlying the transistors and the active areas;

forming a mask overlying the insulating layer;

patterning the mask to define one or more contact plug openings over one or more of the active areas, to define a contact plug/local interconnect hole above a first transistor, a first portion of an immediately adjacent second transistor and a first active area between the first and second transistors, and to define a local interconnect trench over a second portion of the second transistor;

partially removing the insulating layer at the contact plug openings, the contact plug/local interconnect hole, and the local interconnect trench, and removing the insulating layer above the first portion of the second transistor;

forming a dielectric material spacer within the contact plug/interconnect hole to form two contact holes and filling the local interconnect trench;

removing at least a portion of the dielectric material spacer and at least a portion of the dielectric material in the local interconnect trench;

removing a portion of the insulating cap overlying the first portion of the second transistor thereby exposing a first portion of the gate region of the second transistor;

removing any remaining portion of the insulating layer overlying the active areas; and

depositing conductive material within the contact plug openings, the contact plug/local interconnect hole and the local interconnect trench.

26. A semiconductor device having contact plugs and a contact plug/local interconnect, comprising:

a substrate having at least two transistors with gate regions with insulating caps overlying the gate regions, and active areas between adjacent transistors;

one or more contact plugs formed of a conductive material overlying one or more of the active areas;

one or more contact plug/local interconnects formed of a conductive material above a first transistor, a first portion of an immediately adjacent second transistor and a first active area between the first and second transistors, wherein a first portion of the gate region of the second transistor is exposed; and

a dielectric material spacer above the first transistor and immediately underlying the conductive material forming the contact plug/local interconnect.

27. The semiconductor device of claim 26, wherein the transistors are FETs.

28. A semiconductor device having electrical interconnects comprising:

a substrate having two or more transistors with active areas therebetween, the transistors having gate regions wherein a portion of the gate region of a first portion of a first transistor is exposed;

a contact plug/interconnect positioned over a first and a second active area, a second transistor and the first portion of the gate region of the second first transistor thereby electrically connecting the gate region of the first transistor to the first and second active areas;

a local interconnect overlying a second portion of the first transistor; and

a layer of dielectric material overlying an insulating cap overlying the gate region of the first transistor and immediately underlying the local interconnect.

29. The device of claim 28, wherein the dielectric material comprises TEOS or silicon dioxide.

30. The device of claim 28, wherein the transistors are FET transistors.

31. The device of claim 28, wherein the FET transistors are shallow-trench isolated FET transistors.

32. The semiconductor device of claim 28 further comprising one or more contact plugs formed of a conductive material overlying one or more of the active areas.

33. The semiconductor device of claim 28 further comprising a TEOS or silicon dioxide spacer above the second transistor and immediately underlying a portion of the contact plug/local interconnect.

34. A method of forming electrical interconnects and buried bit lines in a semiconductor device comprising:

providing a substrate having two or more transistors with active areas therebetween;

creating an insulating layer overlying the transistors and active areas;

forming a hard mask over the insulating layer;

patterning the hard mask to define cell contacts above the active areas and buried bit lines between the cell contacts;

removing a portion of the insulating layer to form cell contact trenches and buried bit line trenches;

depositing spacers to substantially fill the buried bit line trenches;

removing portions of the insulating layer within the cell contact trenches to expose the active areas underlying the cell contacts;

recess the spacers within the buried bit lines; and

deposit conductive material within the buried bit line trenches and the cell contact trenches.

35. A method of forming electrical interconnects and buried bit lines in a semiconductor device comprising:

providing a substrate having two or more FET transistors with active areas therebetween;

creating an insulating layer overlying the transistors and active areas;

patterning the insulating layer to define cell contacts above the active areas and buried bit lines between the cell contacts;

removing a portion of the insulating layer to form cell contact trenches and buried bit line trenches;

depositing dielectric material to form spacers within the buried bit line trenches and a dielectric layer within the cell contact trenches;

removing the dielectric material and portions of the insulating layer within the cell contact trenches to expose the active areas underlying the cell contacts while recessing the spacers within the buried bit lines; and

depositing conductive material within the buried bit line trenches and the cell contact trenches.

36. A method of forming electrical interconnects and buried bit lines in a semiconductor device comprising:

providing a substrate having two or more shallow-trench insolated transistors with active areas therebetween and word lines traversing the active areas;

creating an insulating layer overlying the transistors, active areas and word lines;

patterning the insulating layer to define cell contacts above the active areas and buried bit lines above shallow trenches of the transistors;

removing a portion of the insulating layer to form cell contact trenches and buried bit line trenches;

depositing dielectric material to form spacers within the buried bit line trenches and a dielectric layer within the cell contact trenches;

removing the dielectric material and portions of the insulating layer within the cell contact trenches to expose the active areas underlying the cell contacts while partially removing the spacers within the buried bit lines; and

depositing conductive material within the buried bit line trenches and the cell contact trenches.

37. The method of claim 36, wherein the spacers comprise TEOS or silicon dioxide.

38. A semiconductor device made according to the process of claim 34.

39. A semiconductor device made according to the process of claim 35.

40. A semiconductor device made according to the process of claim 36.